We Claim:

1. A group write slave comprising:

an identification stage having a first ID input, a second ID input and an ID output, wherein said identification stage includes ID logic circuitry for processing said first ID input and said second ID input;

a select stage having a select input and a select output, wherein said select stage includes select logic circuitry for processing said select input; and

a slave module, wherein said slave module includes a plurality of slave inputs communicated with said select output and said ID output, a plurality of slave outputs and slave logic circuitry for processing said plurality of slave inputs so as to create said plurality of slave outputs.

2. A group write slave according to claim 1, wherein said ID logic circuitry includes an ID comparator and an ID AND gate, wherein said ID comparator is communicated with said first ID input, said second ID input and said ID AND gate, and wherein said ID AND gate is communicated with said first ID input and said slave module.

3. A group write slave according to claim 2, wherein said select logic circuitry includes a group write comparator, an individual select comparator, an OR gate and a select AND gate, wherein said group write comparator and said individual select comparator are communicated with said select input and said OR gate and wherein said select AND gate is communicated with said OR gate, said select input, said ID comparator and said slave module.

4. A group write slave according to claim 2, wherein said ID comparator includes ID comparator logic circuitry which compares said first ID input with said second ID input.

5. A group write slave according to claim 3, wherein said group write comparator includes group write logic circuitry for processing said select input so as to determine whether said group write slave has been selected as a group.

6. A group write slave according to claim 3, wherein said individual select comparator includes individual select logic circuitry for processing said select input so as to determine whether said group write slave has been selected as an individual.

7. A group write slave according to claim 1, wherein said first ID input is communicated with a master so as to allow communication of a first master signal, wherein said first master signal includes slave address information and slave ID information.

8. A group write slave according to claim 1, wherein said second ID input is communicated with a master so as to allow communication of a second master signal, wherein said second master signal includes group write identification information.

9. A group write slave according to claim 1, wherein said select input is communicated with a master so as to allow communication of a third master signal, wherein said third master signal includes group write command information.

10. A group write slave according to claim 1, wherein at least one of said plurality of slave outputs is communicated with a type one status bus.

11. A group write slave according to claim 1, wherein at least one of said plurality of slave outputs is communicated with a type two status bus.

12. A group write slave according to claim 1, wherein at least one of said plurality of slave outputs includes a slave wait signal and a slave rearbitrate signal and is communicated with a type three status bus.

13. A group write slave according to claim 1, wherein at least one of said plurality of slave outputs is responsive to a group wait signal, wherein said group wait signal is generated through a logical operation conducted external to said group write slave.

14. A group write slave design according to claim 1, wherein at least one of said plurality of slave outputs is responsive to a group rearbitrate signal, wherein said group rearbitrate signal is generated through a logical operation conducted external to said group write slave.

15. A sequence alignment logic module comprising:

a plurality of SAL inputs for receiving a plurality of SAL input signals from a plurality of group write slaves;

at least one SAL output for communicating at least one SAL output signal; and

a gated logic portion, said gated logic portion having logic circuitry communicated with said plurality of SAL inputs and said SAL output, wherein said logic circuitry is constructed so as to create said SAL output signal by sequencing and combining said plurality of SAL input signals so as to represent the slowest of said plurality of SAL input signals.

16. A sequence alignment logic module according to claim 15, wherein said plurality of SAL inputs includes a first SAL input and a second SAL input.

17. A sequence alignment logic module according to claim 16, further comprising a first multiplexor having a first multiplexor select input, a first data input, a first GRL data input and a first multiplexor output, wherein said first data input is communicated with said first SAL input and wherein said first GRL data input is communicated with said SAL output port.

18. A sequence alignment logic module according to claim 17, further comprising a second multiplexor having a second multiplexor select input, a second data input, a second GRL data input and a second multiplexor output, wherein said second data input is communicated with said second SAL input and wherein said second GRL data input is forced to a logic zero.

19. A sequence alignment logic module according to claim 16, further comprising a first multiplexor having a first multiplexor select input and a first multiplexor output, wherein when said first multiplexor select input is held to one of either a logic high or a logic low state, said first multiplexor output is equal to said first SAL input and wherein when said first multiplexor select input is held to the other of said logic high or said logic low state, said first multiplexor output is equal to said SAL output.

20. A sequence alignment logic module according to claim 16, further comprising a second multiplexor having a second multiplexor select input and a second multiplexor output, wherein when said second multiplexor select input is held to one of either a logic high or a logic low state, said second multiplexor output is equal to said second SAL input and wherein when said second multiplexor select input is held to the other of said logic high or said logic low state, said second multiplexor output is equal to either of said logic high or said logic low.

21. A method for using a group write slave and a sequence alignment logic module comprising:

obtaining a computing system that employs a master, at least one conventional slave, at least one group write slave, three sequence alignment logic modules, multiplexor logic circuitry and a processor local bus;

selecting said group write slaves so as to cause said group write slave to create a slave response;

applying said slave response to said sequence alignment logic module so as to create a mixed response;

applying said slave response and said mixed response to said multiplexor logic circuitry so as to create a multiplexor response;

performing logical operations on said multiplexor response so as to create a gated OR response having a wait signal and a rearbitrate signal; and

communicating said gated OR response to said master and to said group write slaves.

22. A method according to claim 21, wherein said obtaining a computing system includes obtaining a computing system where said master is communicated with said processor local bus which is communicated with said conventional slave and said group write slaves via a command bus and a shared bus.

23. A method according to claim 21, wherein said obtaining a computing system includes obtaining a computing system wherein said group write slaves are communicated with said sequence alignment logic modules, and wherein said sequence alignment logic modules are communicated with said processor local bus via a type one status bus, a type two status bus and a type three status bus.

24. A method according to claim 21, wherein said selecting said group write slaves include operating said computing system so as to cause said master to communicate slave address information, slave ID information, group ID information, command information and write data information to said group write slaves.

25. A method according to claim 24, wherein said selecting said group write slaves includes comparing said slave address information, said slave ID information, said group ID information and said command information using said group write slaves so as to select said group write slave.

26. A method according to claim 24, wherein said selecting said group write slaves further includes applying said command information and said write data information to said group write slaves so as to create a slave response.

27. A method according to claim 21, wherein applying said slave response to said multiplexor logic circuitry includes generating a multiplexor select signal and communicating said multiplexor select signal to said multiplexor logic circuitry.

28. A method according to claim 23, wherein said performing logical operations includes applying said type three status bus to gated OR logic circuitry so as to produce a plurality said wait signal and said rearbitrate signal.

29. A method according to claim 21, wherein said performing logical operations includes communicating said wait signal and said rearbitrate signal to said group write slaves.

30. A method according to claim 21, wherein said communicating said gated OR response includes communicating said gated OR response and said slave response to said master through said Processor Local Bus.